PVP 14

Code: CS7T4D

IV B.Tech - I Semester – Regular/Supplementary Examinations
March - 2021

ADVANCED COMPUTER ARCHITECTURE
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks
11 x 2 = 22 M

1.

a) Define Parallel Processing.
b) Describe RISC Pipeline.
c) What is signed binary?
d) What are the applications of vector processing?
e) Give the Hardware Implementation of Division Algorithm.
f) Define MIPS Rate.
g) Give the Flynn's classification of Computer Architecture.
h) Define CISC scalar processor.
i) Define Superscalar processor.
j) List various phases of Instruction execution.
k) What is the purpose of Delay Insertion?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Define Vector Processing. Explain memory interleaving in vector processing. 8 M

   b) What is an instruction pipeline? Explain the types of instruction pipeline conflicts with examples. 8 M

3. a) Explain the hardware implementation of Multiplication Algorithm. 8 M

   b) Draw a flowchart for multiplication of two fixed point binary numbers in signed magnitude representation. 8 M

4. a) Explain the various types of Parallel processing models. 8 M

   b) What is the function of SIMD Super computers? 8 M

5. a) Explain the Instruction Set Architecture. 6 M

   b) Explain the RISC scalar processor. 10 M

6. a) Explain Asynchronous and Synchronous model of Linear Pipeline Processor. 10 M

   b) Explain Branch Handling Techniques. 6 M